IN THE CLAIMS

Please add new claims 25-26 as indicated below.

Please amend claims 1, 10, 11, 13, 22, and 23 as follows.

1. (Currently Amended) A processing core comprising:

R-number processing pipelines each comprising N-number of processing paths, wherein each of said R-number of processing pipelines are synchronized to operate as a single very long instruction word (VLIW) processing core, said VLIW processing core being configured to process R x N-number of VLIW sub-instructions in parallel;

wherein each of said R-number of processing pipelines comprises S-number of register files, such that said processing core comprises R x S-number of register files; and

wherein each of said register files comprises Q-number of M-bit wide registers, and wherein said Q-number of registers within each of said register files are either private or global registers, and wherein when a value is written to one of said Q-number of said registers which is a global register within one of said register files, said value is propagated to a corresponding global register in the other of said register files, and wherein when a value is written to one of said Q-number of said registers which is a private register within one of said register files, said value is not propagated to a corresponding register in the other of said register files; and

wherein a Q-bit special register stores bits indicating whether registers in the register files are private registers or global registers, each bit in the Q-bit special register corresponding to one of the registers in the register files.

2. (Original) The processing core as recited in claim 1 wherein said R-number of processing pipelines can be configured to operate independently as separately operating pipelines.

3. (Canceled)

4. (Previously Presented) The processing core as recited in claim 1 wherein each of said R-number of processing pipelines comprises one register file for every two of said N-number of processing paths, such that S=N/2.

5. (Canceled)

6. (Original) The processing core as recited in claim 1, wherein a single VLIW processing instruction comprises R x N-number of P-bit sub-instructions appended together.

7. (Original) The processor chip as recited in claim 6, wherein M=64, Q=64, and P=32.

8. (Previously Presented) The processing core as recited in claim 1 wherein said each of said R-number of processing pipelines comprise an execute stage which includes an execute unit for each of said N-number processing paths, each of said execute units comprising an integer processing unit, a load/store processing unit, a floating point processing unit, or any combination of one or more of said integer processing units, said load/store processing units, and said floating point processing units.

9. (Original) The processing core as recited in claim 8 wherein an integer processing unit and a floating point processing unit share one of said register files.

10. (Currently Amended) The processing core as recited in claim 1 wherein Q=64 ~~, and a 64-bit special register stores bits indicating whether registers in the register files are private registers or global registers, each bit in the 64-bit special register corresponding to one of the registers in the register files~~.

11. (Currently Amended) The processing core as recited in claim 1 wherein a plurality of said register files are connected to a bus, and a value written to a global register in one of said register files connected to the bus is propagated to a corresponding global register in the other of said register files connected to ~~across bus across~~ said bus.

12. (Previously Presented) The processing core as recited in claim 1 wherein a plurality of said register files are connected together in serial, and a value written to a first global register in a first of said plurality of register files is propagated to a corresponding first global register in a second of said plurality of register files connected directly to said first of said plurality of register files.

13. (Currently Amended) In a computer system, a scalable computer processing architecture, comprising:

two or more processor chips, each comprising:

a processing core, including:

R-number processing pipelines each comprising N-number of processing paths, wherein each of said R-number of processing pipelines are synchronized to operate as a single very long instruction word (VLIW) processing core, said VLIW processing core being configured to process R x N-number of VLIW sub-instructions in parallel;

wherein each of said R-number of processing pipelines comprises S-number of register files, such that said processing core comprises R x S-number of register files; and

wherein each of said register files comprises Q-number of M-bit wide registers, and wherein said Q-number of registers within each of said register files are either private or global registers, and wherein when a value is written to one of said Q-number of said registers which is a global register within one of said register files, said value is propagated to a corresponding global register in the other of said register files, and wherein when a value is written to one of said Q-number of said registers which is a private register within one of said register files, said value is not propagated to a corresponding register in the other of said register files;

an I/O link configured to communicate with other of said ~~one~~ two or more processor chips or with I/O devices;

a communication controller in electrical communication with said processing core and said I/O link;

said communication controller for controlling the exchange of data between a first one of said ~~one~~ two or more processor chips and said other of said ~~one~~ two or more processor chips;

wherein said computer processing architecture can be scaled larger by connecting together two or more of said processor chips in parallel via said I/O links of said processor chips, so as to create multiple processing core pipelines which share data therebetween;

wherein a Q-bit special register stores bits indicating whether registers in the register files are private registers or global registers, each bit in the Q-bit special register corresponding to one of the registers in the register files.

14. (Original) The computer system as recited in claim 13 wherein said R-number of processing pipelines can be configured to operate independently as separately operating pipelines.

15. (Canceled).

16. (Previously Presented) The computer system as recited in claim 13 wherein each of said R-number of processing pipelines comprises one register file for every two of said N-number of processing paths, such that S=N/2.

17. (Canceled).

18. (Original) The computer system as recited in claim 13 wherein a single VLIW processing instruction comprises R x N-number of P-bit sub-instructions appended together.

19. (Original) The computer system as recited in claim 18 wherein M=64, Q=64, and P=32.wherein M=64, Q=64, and P=32.

20. (Previously Presented) The computer system as recited in claim 13 wherein said each of said R-number of processing pipelines comprise an execute stage which includes an execute unit for each of said N-number processing paths, each of said execute units comprising an integer processing unit, a load/store processing unit, a floating point processing unit, or any combination of one or more of said integer processing units, said load/store processing units, and said floating point processing units.

21. (Original) The computer system as recited in claim 20 wherein an integer processing unit and a floating point processing unit share one of said register files.

22. (Currently Amended) The computer system as recited in claim 13 wherein Q=64~~, and a 64-bit special register stores bits indicating whether registers in the register files are private registers or global registers, each bit in the 64-bit special register corresponding to one of the registers in the register files~~.

23. (Currently Amended) The computer system as recited in claim 13 wherein a plurality of said register files are connected to a bus, and a value written to a global register in one of said register files connected to the bus is propagated to a corresponding global register in the other of said register files connected to ~~across bus across~~ said bus.

24. (Previously Presented) The computer system as recited in claim 13 wherein a plurality of said register files are connected together in serial, and a value written to a first global register in a first of said plurality of register files is propagated to a corresponding first global register in a second of said plurality of register files connected directly to said first of said plurality of register files.

25. (New) A processing core comprising:

R-number processing pipelines each comprising N-number of processing paths, wherein each of said R-number of processing pipelines are synchronized to operate as a single very long instruction word (VLIW) processing core, said VLIW processing

core being configured to process R x N-number of VLIW sub-instructions in parallel;

wherein each of said R-number of processing pipelines comprises S-number of register files, such that said processing core comprises R x S-number of register files; and

wherein each of said register files comprises Q-number of M-bit wide registers, and wherein said Q-number of registers within each of said register files are either private or global registers, and wherein when a value is written to one of said Q-number of said registers which is a global register within one of said register files, said value is propagated to a corresponding global register in the other of said register files, and wherein when a value is written to one of said Q-number of said registers which is a private register within one of said register files, said value is not propagated to a corresponding register in the other of said register files; and

wherein a plurality of said register files are connected together in serial, and a value written to a first global register in a first of said plurality of register files is propagated to a corresponding first global register in a second of said plurality of register files connected directly to said first of said plurality of register files.

26. (New) In a computer system, a scalable computer processing architecture, comprising:

two or more processor chips, each comprising:

a processing core, including:

R-number processing pipelines each comprising N-number of processing paths, wherein each of said R-number of processing pipelines are synchronized to operate as a single very long instruction word (VLIW) processing core, said VLIW processing core being configured to process R x N-number of VLIW sub-instructions in parallel;

wherein each of said R-number of processing pipelines comprises S-number of register files, such that said processing core comprises R x S-number of register files; and

wherein each of said register files comprises Q-number of M-bit wide registers, and wherein said Q-number of registers within each of said register files

are either private or global registers, and wherein when a value is written to one of said Q-number of said registers which is a global register within one of said register files, said value is propagated to a corresponding global register in the other of said register files, and wherein when a value is written to one of said Q-number of said registers which is a private register within one of said register files, said value is not propagated to a corresponding register in the other of said register files;

an I/O link configured to communicate with other of said two or more processor chips or with I/O devices;

a communication controller in electrical communication with said processing core and said I/O link;

said communication controller for controlling the exchange of data between a first one of said two or more processor chips and said other of said two or more processor chips;

wherein said computer processing architecture can be scaled larger by connecting together two or more of said processor chips in parallel via said I/O links of said processor chips, so as to create multiple processing core pipelines which share data therebetween;

wherein a plurality of said register files are connected together in serial, and a value written to a first global register in a first of said plurality of register files is propagated to a corresponding first global register in a second of said plurality of register files connected directly to said first of said plurality of register files.